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A Study of Resistive Open Fault Detection on Low Power Nanometric ICs

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Abstract

Resistive open fault represents degradation in conductivity within a circuit interconnection. Due to this manufacturing failure occurs in IC interconnection. Such fault causes performance failures and reliability risk. an interconnect-open defects have attracted a significant research effort world-wide to reduce test cost without an affecting the fault coverage-in the context of multi-VDD designs. Recent studies have shown that full open defects can be tested using static test techniques at any VDD setting, as they do not exhibit VDD dependent detectability. On the other hand, the resistive-open defects are better detectable and these elevated at applying multiple VDD settings using various delay test techniques. This paper presents the analysis of various detection methods for resistive open faults. And detectable resistance range versus VDD varies with the test speed also observes. Depending on test speed and small delay faults Multi-VDD is required for detection of ROFs.

Keywords: Resistive Open Faults, Small Delay Faults, Test Speed, Low Power Design, Multi-VDD Test.

INTRODUCTION

Resistive open faults represent degradation in conductivity within a circuit interconnects, due to inevitable manufacturing failures in current and emerging technologies. Such faults cause performance failures and reliability risks whose magnitude is not only voltage sensitive, but also influenced by the electrical characteristics of driving and driven CMOS networks.

To verify that the testing at the gate level of each logic gate in the circuit is functioning properly or not and also to check the interconnections are good. It is the main objective of the gate level test. Resistive opens are a common manufacturing defect that induces faults like voltage dependent delay faults [1] and due to their break like nature it poses potential reliability risks. The resistive open fault effect is distributed and refers to as permanent faults.

The important thing in reducing failures is differentiating of delay failures which are induced by resistive open faults from those induced by other mechanisms. The empirical observations of VDD versus delay pattern for resistive opens compared to other fault mechanisms [2, 3] are given from these techniques. The detectability of Resistive Open Faults and behavior depends on the technological, electrical characteristics of the design and test conditions, as well as the VDD-supply voltages. The comprehensive modeling of the behavior of the open faults and detectability becomes challenging. The detectability of delay fault sometimes may be sensitive to the speed of the test. The behavioral aspects of Resistive Open Fault the conventional models have not considered with respect to VDD.

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Therefore, based on these issues efficient fault detection and testing method, which works with multi VDD has to be developed. The previous work demonstrated due to the supply voltage-dependent delay behavior, by testing at multiple VDD values that the fault coverage could be improved.

Present days the low power IC design that utilizes multiple supply voltage levels need multi-VDD testing could become more convenient for effective testing of resistive open faults. The main aim of this paper is to give the analysis of both behavioral and detect ability aspects of the delay caused by ROF.

2. OPEN RESISTANCE INTERVALS

In this empirical analysis, the optimal detectability provided by VDD value, in different resistance intervals. Then the different resistanc intervals, i_01_ 02_ 03_ _ _ __N_, exhibit the behaviors_Bhv_01__ Bhv_02__ _ _ __ Bhv_N __ respectively. The critical resistance ROi−1–$i$cr, $N \geq i > 1$ separates the consecutive intervals i−1 and i. The intermediate resistance between two consecutive intervals is known as critical resistance ROi−1–$i$cr. The detectability is concerned; the continuous resistance is named into three detectability ranges and it shown in Figure 1. They are gross delay faults, small delay faults, and undetectable delay faults. This proposed model represents those detectability resistance ranges for gross delay faults and small delay faults by the resistance detection threshold. The delays caused by undetected delay faults are very small. So, the undetected delay fault cannot be detected. The gross delay faults are cumulative propagation delay exceeding the longest path delay.

Remaining faults are small delay faults. The major problem is an undetectable delay fault. The given VDD value doesn't not have the capability to detect these faults. The proposed model mainly focusing on undetectable delay faults caused by resistive opens.

The following Figure 2 shows a resistive open fault [ROF] model, here D-driver and S-successor gate, respectively understood from ROTH, and it is found from exhaustive parametric circuit-level simulations. Resistive open can be modeled as a resistor between two unconnected wires.

The open resistance interval [4] assumed as from ROmin to ROmax. With a constant supply voltage, the behavior of fault will be observed that linearly increasing open resistance [RO] value. If the behavior changes from one behavior to another then that can be considered as next interval.If the resistance value at which the propagated delay is equal to TCP (Test Clock Period) is called Open Resistance Detection Threshold (ROTH). The delay can be detected in the range of above period is known as Test Clock Period (TCP). In the same mannerthe full open resistance range will be divided into N number of intervals

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{like 01_ 02_ 03_ _ _ __N}. The behavior of delay with respect to supply voltage will be varying

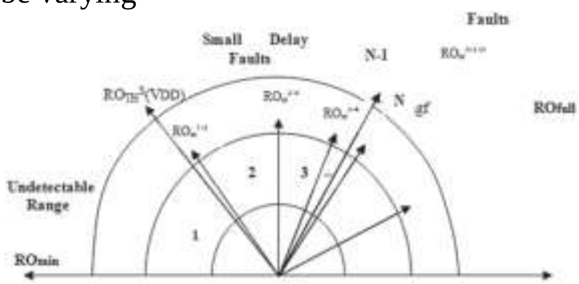

Fig. 1. Open resistance intervals.

Fig. 2. Resistive open defect model.

in different resistance intervals. Then the different resistance intervals, *i*_01_ 02_ 03_ _ _ __*N*_, exhibit the behaviors _*Bhv*_01__ *Bhv*_02__ _ _ __ *Bhv*_*N* __ respectively. The critical resistance RO*i*−1–*i*cr, *N* ≥*i* > 1 separates the consecutive intervals *i*−1 and *i*. The intermediate resistance between two consecutive intervals is known as critical resistance RO*i*−1–*i*cr. The detectability is concerned; the continuous resistance is named into three detectability ranges and it shown in Figure 1. They are gross delay faults, small delay faults, and undetectable delay faults. This proposed model represents those detectability resistance ranges for gross delay faults and small delay faults by the resistance detection threshold. The delays caused by undetected delay faults are very small. So, the undetected delay faults cannot be detected. The gross delay faults are cumulative propagation delay exceeding the longest path delay. Remaining faults are small delay faults. The major problem is an undetectable delay fault. The given VDD value doesn't not have the capability to detect these faults. The proposed model mainly focusing on undetectable delay faults caused by resistive opens. The following Figure 2 shows a resistive open fault [ROF] model, here D-driver and S-successorgate, respectively.

3. LITERATURE SURVEY

Last two decades, the active research area are minimizing the power consumption through the use of low power design techniques and it is motivated by the portable and hand-held devices application market.

In this section summarizes the recent research on test techniques for resistive interconnect open defect and an impact of voltage setting on their testability. The timing dependent effects described from the resistive opens and these are tested using delay tests. The delay fault testing is used to detect the defects that create additional than expected delay and thereby cause a malfunction of the Integrated Circuits. By using this delay fault testing, a defect is detectable only when it causes longer delay than that of the longest path in a fault free design. It was shown in that the majority of tested paths show less than one-third delay in comparison to that of the longest path.

Therefore a defect in any of these shorter paths can only be detected if it causes higher delay than that of the longest path in the design.

In brief, an interconnect-open defects have attracted a significant research effort world-wide to reduce test cost without an affecting the fault coverage-in the context of multi-VDD designs. Recent studies have shown that full open defects can be tested using static test techniques at any VDD setting, as they do not exhibit VDD dependent detectability. On the other hand, the resistive-open defects are better detectable and these elevated at applying multiple VDD settings using various delay test

4. ROFs DETECTION METHODS

Renovell [5] proposed Specific ATPG method for detection Resistive Open Fault. It considers predictable resistance value as a node. It doesn't specify the exact ROF value. March Test used for detection of Resistive Open Fault, Dilillz [6]. This test gives comparison of tests to detect ROFs in SRAM Cell. Then next Resistive Open Fault detection method stuck-at and transition fault testing by Czutro [7]. It detect only small delay fault.

Multiple-VDD Test gave Khursheed [8] for detection ROFs in Integrated Chips. He focused on Resistive BridgeFaults, just given three different voltage settings (0.8 V, 1.0 V, 1.2 V) required for this test. Next elaborated this Multiple-VDD Test by Ali [9]. It presents a parametric, Voltage-aware resistive open fault model for ROFs.Single-VDD Test presented Yang, for detection of ROFs It doesn't minimize possibilities of test escapes.

Recently Mohammadat recognized multi-VDD tests could be required, depending on the test speed for detection Resistive Open Faults in low power nanometric ICs. But it just minimizes possibilities of test escapes only 25%.Various methods method for detection of ROFs in specific ICs are, first sub-micron technology, Tahoori [10].

Testing for Resistive Open Defects in FPGAs. DFT by Haron [11] for Resistive Open Fault in DRAM. It is applicable to only DRAMs. Montanes poses Yield Evaluation Monitor method for detecting weak open-line defects.

Define resistance ranges of various ROFs like Weak Open—[1 M_–10 M_] Strong Open—[10 M_–1 G_].

IDDT test also used for detection of ROFs, Changgeng Yu. It results some resistive open defects do not cause failure of the circuits function immediately. It ignores these ROFs.

5. CONCLUSION

The present study has focused on detection of Resistive Open Faults. Literature survey gives knowledge on testing methods for detection ROFs. The behavior of delay caused by ROF will be analyzed as a function of set of supply voltages VDD. The intend is to continue this study of Resistive Open Faults by analyzing more carefully their effects on Low Power Nanometric ICs and an invention of new testing method.

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